Optical Network on Chip in 3D Architectures

Sébastien Le Beux

Ecole Centrale de Lyon, France
contact : Sebastien.Le-Beux@ec-lyon.fr

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Outline

1. Introduction
2. Optical Network on Chip
3. Layout Guidelines
4. Experimental Results
5. Conclusion and Future Work
MPSoC Design Trends

• Multiple layers $\rightarrow$ multiple technologies (3D integration + heterogeneity):
  • computation $\rightarrow$ electrical layer
  • communication $\rightarrow$ optical layer
MPSoC Design Trends

- Multiple layers $\rightarrow$ multiple technologies (3D integration + heterogeneity):
  - computation $\rightarrow$ electrical layer
  - communication $\rightarrow$ optical layer

- Optical Network on Chip (ONoC) characteristics
  - high throughput: *Wavelength Division Multiplexing, WDM*
  - long range communications (chip scale)
  - low latency
Related Work and Contribution

- Mesh [4], multistage [2], fat-tree [5], torus [12]
  - waveguide crossings $\rightarrow$ losses (about 0.3dB for the multistage)
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  - no waveguide crossings and simpler layout
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Electrical NoC

- resource sharing
+ number of resources
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**Electrical NoC**

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- number of resources

**Optical NoC**

+ no contention in ONoC
- shared access, number of resources
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Electrical NoC
- resource sharing
+ number of resources

Optical NoC
+ no contention in ONoC
- shared access, number of resources

ORNoC : Optical Ring Network on Chip
+ zero contention (WDM + virtual waveguide partitioning)
+ optimal number of resources
Optical Network Interface (ONI)

- Operation mode:
  - ejection
  - pass through
  - injection
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W. Bogaerts et al.,
IEEE JSTQE, 16(1), 33 (2010)

L. Vivien et al.,
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L. Vivien et al., Optics Express, 17, 6252 (2009)

J. Van Campenhout et al., IEEE PTL, 20, 1345 (2008)
ORNoC in 3D Architecture

Signal Direction

ONI
waveguide
ORNoC in 3D Architecture

ONI waveguide
ORNoC in 3D Architecture

- Communication hierarchy:
  - Electrical NoC → intra-layer communication
  - ORNoC → inter-layer communication
ORNoC in 3D Architecture

- Communication hierarchy:
  - Electrical NoC → intra-layer communication
  - ORNoC → inter-layer communication
How to configure ONI?

- ORNoC benefits: contention free, scalable, low power
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- ORNoC benefits: contention free, scalable, low power
- Need for...
  - (high level) layout guidelines
  - ONI area overhead estimation
  - regularity and reuse (x, y and z dimensions)
Layout Guidelines

- **Objective**: take benefits from the regularity of ORNoC
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Layout Guidelines

• **Objective**: take benefits from the regularity of ORNoC

• **VC_{area}**
  - elementary footprint to consider (worst case)
  - highly technology dependent
Layout Examples

\[ WL \]: number of wavelengths
**Layout Examples**

**WL** : number of wavelengths

photonic layer

electrical layer

**WG** : number of waveguides

two waveguides

photonic layer

electrical layer
Layout Examples

**WL**: number of wavelengths

**WG**: number of waveguides

**L**: number of electrical layers

- **photonic layer**
- **electrical layer**
- **shifted identical electrical layers**
- **area allocated to propagate vertical connexions**
- **two waveguides**
Area overhead estimation

• Area used to implement each ONI:

\[ \text{ONI}_{\text{area}} = 2 \times \text{VC}_{\text{area}} \times \text{WL} \times \text{WG} \]

• Area overhead used to “propagate” ONI:

\[ \text{ONI}_{\text{area\_overhead}} = \text{ONI}_{\text{area}} \times (L - 1) \]
Area overhead estimation

- Area used to implement each ONI:
  \[ ONI_{area} = 2 \times VC_{area} \times WL \times WG \]

- Area overhead used to "propagate" ONI:
  \[ ONI_{area\_overhead} = ONI_{area} \times (L - 1) \]

- Total area obtained by considering the number of ONI per layer
Area overhead estimation

**Assumptions:**
- $V_{C_{\text{area}}}$?
- CMOS driver: $8.5 \mu m \times 9.5 \mu m$ (350 $\mu$A current threshold [13] and 0.13 $\mu m$ CMOS technology [7])
- TSV: $pitch \approx 5 \mu m \times 5 \mu m$ [3]
- Photonic receiver: less than $20 \mu m^2$ [6]
- CMOS receiver footprint < CMOS driver footprint [7]
- Photonic transmitter: microdisk laser radius (7.5 $\mu m$ [13]), microdisk resonator radius (10 $\mu m$), waveguide diameter (1 $\mu m$ [8])
Area overhead estimation

• Assumptions:
  • $VC_{area} = 10 \mu m \times 18.5 \mu m$
  • initial electrical die size : $491 mm^2$ for 256 cores [11]
  • 2 electrical layers
Area overhead estimation

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- 32 ONIs $\rightarrow 4 \times 4$ ONIs per electrical layer
  • each ONI is shared by 16 cores
  • 0.5% area overhead
  • reliability-complexity design tradeoff

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Conclusion and Future Work

• ORNoC
  • suitable for 3D architectures (communication hierarchy)
  • layout guidelines → regularity in x, y and z dimensions
  • ONI area overhead estimation
    • e.g. : 36 ONIs, 2 electrical layers → 0.5% area overhead

• Future work
  • loss modeling and estimation
  • laser power control
  • SERDES footprint
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Optical Network Interface (ONI)

- Operation mode:
  - ejection
  - pass through
  - injection

![Diagram of ONI components]

Signal direction

- laser
- on-chip laser
- photodetector
- microresonator
How to configure ONI?

- Which waveguide partition?
- Which wavelength?
How to configure ONI?

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How to configure ONI?

- ORNoC benefits: contention free, scalable, low power

Waveguide
Optical layer (ORNoC)
Electrical layers
How to configure ONI?

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- Communication hierarchy:
  - Electrical NoC → *intra-cluster* communication
  - ORNoC → *inter-cluster* communication

Connectivity Matrix:

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- 0 → no communication
- 1 → communication required